Docket No.: LGS/S-0030A PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	**EXPEDITED PROCEDURE UNDER 37 C.F.R. §1.116**
Joo-Hyong LEE	
Serial No. 09/955,288	Group Art Unit: 2815
Confirm. No.: 9373	Examiner: Jose R. Diaz
Filed: September 19, 2001	
For: LATCH-UP RESISTANT CMOS STRUCTURE	

#9/Req for reconsn w/ Attach. AMDann 2/27/03

REQUEST FOR RECONSIDERATION

BOX AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

In reply to the Office Action dated November 20, 2002, please consider the following remarks:

Claims 1-5 and 11-25 are pending in this application. Reconsideration in view of the following remarks is respectfully requested.

I. 35 U.S.C. §102(b)/(e) (Farrenkopf and Zunino)

The Office Action rejects claims 1-4, 13-18, 21-22 and 24-25 under 35 U.S.C. §102(e) over Farrenkopf et al. (U.S. Patent No. 5,899,714) (hereinafter Farrenkopf). Additionally, the Office Action rejects claims 1-2, 12, 15-16, and 21-24 under 35 U.S.C. §102(b) over Zunino

(U.S. Patent No. 4,646,124). Since the references fail to disclose or suggest all the features of the claims, the rejection is respectfully traversed.

Applicant respectfully submits that the Farrenkopf reference appears to disclose integrated circuits with barrier regions between either a substrate and an epitaxial layer or an epitaxial layer and a well. See Figure 2.3 of Farrenkopf.

Additionally, Applicant respectfully submits that similar to Farrenkopf, the Zunino reference appears to disclose, as illustrated in Figures 1 and 2, a substrate 10 with a buried layer 40, a well region 18, and epitaxial layers 11A, 11B, and 11C.

Farrenkopf and Zunino both appear to disclose buried layers/regions between an interface of an epitaxial layer and a substrate and a contact zone/region. We note that one of ordinary skill in the art would know that a well is different from an epitaxial layer as an epitaxial layer is usually provided with a primary substrate to grow high purity silicon of controlled thicknesses with accurately determined dopant concentrations distributed homogeneously throughout the layer, wherein wells are formed above the epitaxial layer. See pages 124-125 of Principles of CMOS VLSI Design (Appendix A).

Furthermore, that the well is located above the epitaxial layer and as such the epitaxial layer is clearly not the same layer as the well. As such, in both Farrenkopf and Zunino an interface between the well and the substrate does not exist, but rather two other interfaces exist - one interface between the epitaxial layer and the well and another interface between the epitaxial layer and the substrate, therefore at least claims 1, 15, and 24 are allowable.

For at least the reasons set forth above, Applicant respectfully submits that claims 1, 15 and 24 are allowable. Claims 2-4 and 12-14 depend from claim 1, claims 16-18, 21, and 22 depend from claim 15, and claim 25 depends from claim 24, and are allowable for at least the same reasons, as well as their added features and the combinations thereof. Withdrawal of the rejection is respectfully requested.

II. 35 U.S.C. §102(e) (Wong)

The Office Action rejects claims 1-2, 4-5, and 11-25 under 35 U.S.C. §102(e) over Wong (U.S. Patent No. 6,232,165). Since Wong fails to disclose or suggest all the features of the claims, the rejection is respectfully traversed.

Applicant respectfully submits that the Wong reference appears to disclose a MOS transistor with buried guard rings to prevent latch-up in a complementary metal-oxide semiconductor integrated circuit. In Figure 1, the IC device 2 includes a p-type semiconductor substrate 4, along with well regions 6, 8, and doped regions 16, 22.

Further, Applicant respectfully submits that the buried layer as claimed in the application in claims 1, 15, and 24, is separate from the contact region, which is different from Wong which discloses a doped diffusion region 16, 22 extending from a surface of a well region 6, 8 around and beneath the proximate shallow trench isolation regions 14-2, 14-3, 14-4, and 14-5 to form a single doped diffusion region. As illustrated on page 137 of Principles of CMOS VLSI Design (see Appendix A), to form a bipolar transistor, a starting material substrate is lightly doped to

form a buried layer, then a epitaxial layer is grown thereon, and wells are then diffused so that they join in the middle of the epitaxial layer. Therefore, Wong, similar to Farrenkopf and Zunino, fails to disclose or suggest at least the feature of claims 1, 15, and 24.

Finally, also with respect to the Wong reference, the diffusion regions 16, 22 of Wong are not in fact buried layers, as recited in the claims of the claimed invention. Rather, the diffused regions, as illustrated in Figure 1 of Wong, are contact regions and not buried layers. Therefore, claims 1, 15, and 24 are allowable.

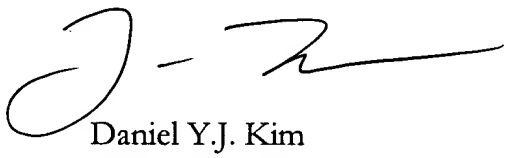
For at least the reasons set forth above, Applicant respectfully submits that claims 1, 15 and 24 are allowable. Claims 2, 4, 5, and 11-14 depend from claim 1, claims 16-23 depend from claim 15, and claim 25 depends from claim 24, and are allowable for at least the same reasons, as well as their added features and the combinations thereof. Withdrawal of the rejection is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, **Laura L. Lee**, at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



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Enc: Appendix A

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